CLAIMS

What is claimed is:

1. An electronic system comprising:

a first memory module having a first memory array and a first buffer logic coupled to the first memory array; and

a second memory module having a second memory array and a second buffer logic coupled to the second memory array, wherein the second buffer logic is further coupled the first buffer logic of the first memory module, and transmits a test pattern to the first memory module to carry out a test of the first memory module independently of the memory controller.

2. The electronic system of claim 1, further comprising:

a memory controller coupled to the second buffer logic; and

a processor coupled to the memory controller to execute instructions stored in the second memory array of the second memory module under the control of the memory controller.

3. The electronic system of claim 2, wherein the memory controller transmits a command to the second buffer logic under the control of the processor to cause the second buffer logic to carry out a test of the first memory module.

4. The electronic system of claim 3, further comprising a memory bus coupling together the memory controller, the first memory module and the second memory module, and wherein the test pattern is transmitted across the memory bus.

5. The electronic system of claim 1, further comprising a point-to-point bus coupling the second buffer logic of the second memory module to the first buffer logic of the first memory module, wherein the test pattern is transmitted by the second buffer logic across the point-to-point bus to the first buffer logic.

6. The electronic system of claim 1, further comprising a test source coupled to the second buffer logic, wherein the test source transmits a command to the second buffer logic to cause the second buffer logic to carry out a test of the first memory module.

7. The electronic system of claim 6, further comprising a serial bus coupling the second buffer logic to the test source, wherein the command is transmitted by the test source across the serial bus to the second buffer logic.

8. The electronic system of claim 6, wherein the test pattern is received by the second buffer logic from the test source and wherein the second buffer logic stores the test pattern in the second memory array in preparation for transmitting the test pattern to the first buffer logic of the first memory module.

9. The electronic system of claim 1, wherein the test pattern is generated by the second buffer logic in response to commands received by the second buffer logic and wherein the second buffer logic stores the test pattern in the second memory array in preparation for transmitting the test pattern to the first buffer logic of the first memory module.

10. The electronic system of clam 1, wherein the test pattern incorporates commands for the first buffer logic to carry out.

11. The electronic system of claim 10, wherein the test pattern incorporates a deliberately created error to elicit an expected action on the part of the first memory module upon encountering the deliberately created error.

12. The electronic system of claim 1, further comprising an analysis module having a third buffer logic having an interface to couple the third buffer logic to an analysis device, wherein the analysis module is interposed between the second buffer logic and the first buffer logic such that the second buffer logic is coupled to the third buffer logic and the third buffer logic is coupled to the first buffer logic, and the test pattern transmitted by the second buffer logic to the first buffer logic passes through the third buffer logic.

13. The electronic system of claim 12, further comprising:

a first point-to-point bus coupling the first buffer logic of the first memory module to the third buffer logic; and

a second point-to-point bus coupling the second buffer logic of the second memory module to the third buffer logic.

14. The electronic system of claim 12, wherein the third buffer logic provides an indication to an analysis device of the transmission of the test pattern by the second buffer logic to the first buffer logic, and wherein the third buffer logic provides an indication to an analysis device of a signal transmitted by the first buffer logic in response to the carrying out of a test by the second buffer logic and indicating a status of the test.

15. The electronic system of claim 12, wherein all three of the first buffer logic, the second buffer logic and the third buffer logic are integrated circuits of substantially

similar design, and wherein the interface of the third buffer logic to couple the third buffer logic to an analysis device is of substantially the same design as both a corresponding interface of the first buffer logic to couple the first buffer logic to the first memory array, and a corresponding interface of the second buffer logic to couple the second buffer logic the second memory array.

16. A buffer logic comprising:

a first point-to-point bus interface;

a second point-to-point bus interface;

an interface to a memory array; and

test logic to transmit a test pattern through the first point-to-point interface to carry out a test of a memory module in response to the buffer logic receiving a command.

17. The buffer logic of claim 16, wherein the test logic stores the test pattern in a memory array coupled to the memory interface so as to queue the test pattern in preparation for being transmitted.

18. The buffer logic of claim 16, further comprising an interface to a configuration bus to which a test source may be attached, and from which the command may be received by the buffer logic from the test source.

19. The buffer logic of claim 18, in which the buffer logic receives the test pattern from the test source.

20. The buffer logic of claim 18, in which the buffer logic generates the test pattern in response to at least one test command from the test source.

21. The buffer logic of claim 16, wherein the buffer logic is an integrated circuit attached to a circuitboard of a first memory module to which memory ICs are also attached that form a first memory array to which the buffer logic is coupled.

22. The buffer logic of claim 21, wherein the first memory module is releasably connected to a circuitboard to which a second memory module is electrically coupled, thereby electrically coupling the first and second memory modules, and wherein the buffer logic transmits the test pattern to the other memory module.

23. The buffer logic of claim 22, wherein the buffer logic transmits the test pattern to test another buffer logic within the second memory module.

24. The buffer logic of claim 22, wherein the buffer logic transmits the test pattern to test the second memory array.

25. A method comprising:

coupling a first buffer logic that is coupled to a first memory array and a second buffer logic that is coupled to a second memory array to a third buffer logic; and

coupling a test source to the first buffer logic;

transmitting a command to the first buffer logic to cause the first buffer logic to transmit a test pattern through the third buffer logic to the second buffer logic.

26. The method of claim 25, further comprising storing a test pattern in the first memory array in preparation for transmitting the test pattern to the second buffer logic.

27. The method of claim 25, wherein the coupling of the first buffer logic to the third buffer logic comprises creating a first point-to-point bus between the first buffer

logic and the third buffer logic, and the coupling of the second buffer logic to the third buffer logic comprises creating a second point-to-point bus between the second buffer logic and the third buffer logic.

28. The method of claim 25, further comprising intercepting a signal received by third buffer logic from the second buffer logic during a test transmitting an indication of the receipt of the signal by the third buffer logic to an analysis device coupled to the third buffer logic.

29. The method of claim 25, further comprising:

placing the first buffer logic into a virtual host mode in which the first buffer logic is able to transmit a test pattern to the second buffer logic;

placing the second buffer logic into a normal operating mode in which the second buffer logic would normally be placed to allow a memory controller to store data to and retrieve data from the second memory array; and

placing the third buffer logic into an analysis mode in which the third buffer logic passes on the test pattern transmitted by the first buffer logic to the second buffer logic, and in which the third buffer logic intercepts a signal received from the second buffer logic during testing and transmits an indication of the receipt of the signal to an analysis device.